REMARKS

35 U.S.C. § 112

In paragraph 2 of the Office action, claims 1-2 and 4-6 stand rejected under 35 U.S.C. § 112. The amendment to claim 1 is believed to address the examiner's concern.

35 U.S.C. § 103

In paragraph 4 of the Office action, claims 1-2, 3-7, 9, 20, and 23-25 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Silvestri (U.S. 6,385,129) in view of Cranford, Jr. et al. (U.S. 2005/0111536, hereinafter "Cranford"). Applicants respectfully traverse this rejection.

In the Office action, the examiner first notes a structural similarity between the system disclosed in Silvestri and the system claimed in claims 20 and 23-25. The examiner then notes that Silvestri does not perform the following:

> Select a first group of bit lines from the bus to carry a first plurality of data patterns;
>
> Select at least one of the remaining bit lines from the bus not within the first group to carry a second plurality of data patterns;
>
> Transmit the first plurality of data patterns on [a] . . . selected one of the plurality of bit lines in the data bus; and
>
> Transmit the second plurality of data patterns on . . . one or more of the plurality of bit lines other than the selected bit line.

In essence, the examiner admits that Silvestri does not disclose any of the claimed configuration of the memory controller of system claim 20 or any of the steps of the method claims. The examiner seeks to overcome that shortcoming by asserting that "the system of Silvestri can perform these method steps (See Fig. 5, col. 5, lines 57-67 to col. 6, lines 1-3)." That portion of Silvestri provides as follows:

> FIG. 5 shows a system 500 according to the invention. System 500 includes a processor 502, and memory device 504. Memory 504 represents memory 100, which is shown and described in FIGS. 1 and 2. Processor 502 can be a microprocessor, digital signal processor, embedded processor, microcontroller, or the like. In addition other devices such as an input/output device 503 and graphic device 509 are included in system 500. In one embodiment of FIG. 5, memory device 504 is formed inside a chip 505, which has a plurality of pins 507 located outside of chip 505. Pins 507 represent lines 241, 242 and 243 shown in FIG. 2. Processor 502 and memory device 504 communicate using address signals on ADDRESS lines 511, control signals on CONTROL lines 513, and data signals on DATA lines 512.

As can be seen from the block quote, Silvestri does not suggest performing the missing method steps. That the apparatus of Silvestri *could be* operated in a manner so as to perform the recited method steps is not the test for obviousness. Applicants have not claimed a method which cannot be performed on existing hardware. Applicants have claimed a method, and in the case of claim 20, a system having a memory controller configured to perform the method, which was not known and would not have been obvious in view of the prior art.

Next, the examiner argues that Cranford discloses a serial presence detect circuit and other components able to generate a pseudo random bit sequence PRBS. "This bit sequence can be used for further tests." It is abundantly clear, however, that Cranford has a serial transmission *line*. Paragraph [0064] of Cranford provides in part:

> [0064] The transmission line or transmission channel 3 used in such a serial link application might be typically a single wire, a differential wire pair or an optical channel including laser driver and photo receiver.

Note also Fig. 2 of Cranford which shows the output of the serializer as SD, which means serial data.

> [0067] With the help of a switching unit 1.3, e.g. an OR gate, either the serialized data SD or the pseudo random bit sequence PRBS is directed to a pre-emphasis unit 1.4 which is also a part of the transmitter 1.

Even if the teachings of Cranford are combined with the teachings of Silvestri, the resulting device would, per Cranford, use the serializer to serialize the bit stream so that it could be driven over serial transmission channel 3. Thus, there is no teaching or suggestion in either of the references for transmitting a first one of a plurality of test bits on a selected one of a plurality of bit lines in a bus and further transmitting a second one of a plurality of test bits on one or more of a plurality of bit lines other than the selected bit line. For that reason, it is respectfully submitted that claims 20 and 23-25 are in condition for allowance.

At the bottom of page 4 of the Office action, method claims 1-2, 4-7, and 9 "are rejected under a similar rationale as set forth in the system claims 20 and 23-25." Therefore, the arguments set forth above are equally applicable to claims 1-2, 4-7, and 9. For that reason, it is believed that claims 1-2, 4-7, and 9 are in condition for allowance.

In paragraph 5 of the Office action, claims 10-19 and 21-22 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Silvestri in view of Cranford, as applied to claim 20, and further in view of Enstrom (U.S. 5,530,895). However, with respect to independent claims 10 and 16, as stated at the bottom of page 5 of the Office action:

> As per claims 10 and 16-18, these claims are rejected under similar rationale as set forth in [the rejection of] claim [*sic* claims] 20-22.

It is noted that claims 10 and 16 contain similar language regarding the transmitting of one of a plurality of signals on a selected one of a plurality of bit lines in a bus and transmitting on one or more of the plurality of bit lines other than the selected bit line one of a plurality of signals. Therefore, for the reasons set forth above, it is believed that independent claims 10 and 16 are in condition for allowance.

Because it is applicants' position that all of the independent claims are in condition for allowance, arguments in favor of the patentability of the dependent claims are not set forth at this time. Applicants reserve the right to submit arguments in favor of the patentability of the dependent claims at a later date should that become necessary.

Applicants have made a diligent effort to place the instant application in condition for allowance. Accordingly, a Notice of Allowance for pending claims 1-2, 4-7, and 9-25 is respectfully requested. If the examiner is of the opinion that the instant application is in condition for disposition other than through allowance, the examiner is respectfully requested to contact applicants' attorney at the telephone number listed below.

Respectfully submitted,

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